Session 13 Overview

Optical Communication

Chair: Larry DeVito, Analog Devices, Wilmington, MA

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Communication using light signals over optical fiber holds great promise to lower costs for data transport over both short and long distances. The huge bandwidth and favorable physical characteristics of optical fiber beg to be exploited: in telecom networks, transmitting high-data-rate signals over long distances becomes practical, and in computer systems, high-capacity interconnect, free-from electromagnetic interference and awkward bulky copper cables, is enabled by parallel optics. However, practical details limit cost-effective commercial solutions. In this session, several advances in the practical art of sending and receiving optical signals are presented. Inevitably, such advances will lead to exciting new cost-effective telecom services and higher-performance computer systems.

The 10Gb/s XFP transceiver in Paper 13.1 covers many protocol data rates. The receiver removes jitter from signals and thus eases the task of other components in the system. Also, the transmitter removes jitter from the host system and creates a low-noise output. This dramatic jitter filtering is enabled by a dual-loop DLL/PLL architecture: this is the first use of this architecture at 10Gb/s.

The multi-chip solution of AFE and digital equalizer ICs in Paper 13.2 is the first 10Gb/s MLSE receiver. A Viterbi detector is used to combat dispersion and nonlinearity in OC-192 metro and long-haul links, resulting in 2200ps/nm of dispersion compensation, approximately doubling the link distance.

To guarantee system reliability, redundant clocks are commonly required for communication networks. In the past, switching two redundant clocks has required bulky and costly components. The circuit presented in Paper 13.3 is a simple cost-effective solution which avoids short-term phase-transients and thus maintains timing integrity in the network.

In Paper 13.4, a negative impedance is used to increase gain to compensate the deleterious effects of both photodiode and ESD parasitic capacitances in a 1.25Gb/s fiber-optical transimpedance amplifier.

A fully monolithically integrated optical receiver including a photodiode with amplifier and additional signal processing which extends the bandwidth and improves the sensitivity is described in Paper 13.5. The enhanced performance, obtained from the photodiode structure, allows high reverse voltage and also shields carriers generated in the substrate from being collected in the signal path.

The first 10Gb/s burst-mode laser driver with both average power and the extinction ratio control is presented in Paper 13.6. Previous laser drivers only applied single-loop automatic power control. However, signal fidelity degrades because the extinction ratio was not adequate due to temperature and aging effects in the laser. This chip is an important step towards building low-cost high-speed burst-mode packet-based networks.

The chip presented in Paper 13.7 promises to dramatically reduce the cost of optical interconnects by monolithically integrating both photonic and electronic components on a standard SOI CMOS process. An optical modulator is described that matches the velocity of electric and optical waves in a waveguide. Also a WDM multiplexor/demultiplexor uses a similar structure to calibrate optical-path lengths to improve channel separation in an arrayed waveguide grating.

In Paper 13.8, a 10.3Gb/s VCSEL driver is integrated with a complete Ethernet transceiver in a standard 0.13μm CMOS process. A low supply voltage of 1.2V is enabled by using two signal paths which are combined in transmission lines to drive a VSCEL differentially. The resulting optical eye exceeds the 10Gb/s Ethernet mask by 35%.

The 10Gb/s burst-mode limiting amplifier, presented in Paper 13.9, extends the dynamic range by a factor of five beyond results previously obtained. Valid data is obtained in less than 1ns. The optimum tap in a cascade of gain stages is selected by monitoring the signal amplitude throughout the cascade.

13.1 A 9.95 to 11.1Gb/s XFP Transceiver in 0.13µm CMOS **8:30 AM**
J. Kenney, Analog Devices, Somerset, NJ

A 9.95 to 11.1Gb/s transceiver in 0.13µm CMOS for XFP modules is presented. The CDR uses a dual-loop DLL/PLL to exceed SONET jitter specifications. A half-rate binary phase detector with a 2:1 serializer implements full-rate I/O. Dispersion jitter from 9.5 inches of FR4 is equalized resulting in random jitter(rms) under 4mUI. Power consumption is 800mW.

13.2 An MLSE Receiver for Electronic-Dispersion Compensation of OC-192 Fiber Links **9:00 AM**
J. Ashbrook, Intersymbol Communications, Champaign, IL

A 9.953 to 12.5Gb/s MLSE receiver consisting of an AFE IC in a 0.18µm 3.3V f_t=75GHz, and a digital IC in a 0.13µm 1.2V CMOS is presented. The AFE IC features a 7.5GHz 40dB VGA, a 4b 12.5GS/s ADC, a dispersion-tolerant clock-recovery unit, and a 1:8 DEMUX. The digital IC implements an 8-parallel, delayed recursion MLSE architecture and a non-linear channel estimator. The 4.5W receiver meets the SONET jitter specifications with 2200ps/nm of dispersion at BER=10^{-4}.

13.3 A Monolithic Low-Bandwidth Jitter-Cleaning PLL with Hitless Switching for SONET/SDH Clock Generation **9:30 AM**
D. Wei, Silicon Laboratories, Austin, TX

A single-chip jitter-cleaning PLL with hitless switching is presented. By utilizing the mostly-digital phase build-out technique, the steady-state output phase step after switching is bounded within 200ps. At the loop bandwidth of 800Hz, the maximum output phase transient slope is <4.5ns/ms. The jitter generation is 0.8ps in the OC48 band and 0.4ps in OC192 band. The 16.32mm^2 chip is fabricated in a 0.25µm standard CMOS process and consumes 350mW at 3.3V.

13.4 A 24mW 1.25Gb/s 13kΩ Transimpedance Amplifier Using Active Compensation **10:15 AM**
C-M. Tsai, National Chiao Tung University, Hsinchu, Taiwan

A transimpedance amplifier using active compensation is demonstrated to achieve 3x bandwidth enhancement in a 0.35µm CMOS technology. At a BER of 10^{-12}, the measured dynamic range is -29.5 to 0dBm at 1.25Gb/s. The differential transimpedance gain is adjustable from 500Ω to 13kΩ. The IC consumes 24mW from a 3V supply.

13.5 11Gb/s Monolithically Integrated Silicon Optical Receiver for 850nm Wavelength **10:30 AM**
R. Swoboda, A3PICs, Vienna, Austria

A monolithically integrated optical receiver is realized in a modified silicon 0.5µm BiCMOS process with f_T=25GHz that contains a pin photodiode. At a wavelength of 850nm, a BER of 10^{-9}, a PRBS of 2^{31}-1, the receiver has sensitivities of -10.8dBm, -10.1dBm, and -8.9dBm for data rates of 8Gb/s, 10Gb/s, and 11Gb/s, respectively.

13.6 A 10Gb/s Burst-Mode/Continuous-Mode Laser Driver with Current-Mode Extinction-Ratio Compensation Circuit
D-U. Li, Industrial Technology Research Institute, Hsinchu, Taiwan **10:45 AM**

A burst/continuous-mode laser driver for 10Gb/s Ethernet PONs is implemented in a 0.18µm CMOS process. With a dual-loop current-mode control circuit, the driver automatically compensates the extinction ratio of the laser output. Under burst-mode operation, the laser turn on/off time is <3ns.

13.7 A 10Gb/s Photonic Modulator and WDM MUX/DEMUX Integrated with Electronics in 0.13µm SOI CMOS **11:15 AM**
A. Huang, Luxtera, Carlsbad, CA

Monolithic integration of both photonic and electronic components operating at 10Gb/s in a 0.13µm SOI CMOS process for PowerPC processors is presented. A modulator uses free carrier plasma dispersion in a reverse-biased PIN optical phase shifter in a Mach-Zender interferometer. An AWG demultiplexer uses a forward-biased PIN phase shifter to compensate the optical path length improving the channel separation.

13.8 An Integrated VCSEL Driver for 10Gb Ethernet in 0.13µm CMOS **11:45 AM**
S. Verma, Aeluros, Mountain View, CA

A 10.3Gb/s VCSEL driver is integrated with a complete Ethernet transceiver in a standard 0.13µm CMOS process. When driving a VCSEL differentially, the resulting optical eye exceeds the 10Gb/s Ethernet mask by 35%. Intended for short-reach applications, the driver dissipates 85mW from 1.2V and occupies 0.15mm^2.

13.9 A 10Gb/s Burst-Mode Adaptive Gain Select Limiting Amplifier in 0.13µm CMOS **12:00 PM**
M. Nogawa, NTT, Atsugi, Japan

A 10Gb/s burst-mode limiting amplifier is developed in a 0.13µm CMOS process. An adaptive gain-selection technique achieves a settling time of 0.8ns and a wide input dynamic range of 28dB, which is five-times wider than that of previous work at 10Gb/s.